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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
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EXAMINER	
VAN, LUAN V	

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MIN-LUNG HUANG, CHI-LONG TSAI, CHAO-FU WENG and CHING-HUEI SU

Appeal 2008-3343
Application 10/710,020
Technology Center 1700

Decided: September 11, 2008

Before THOMAS A. WALTZ, JEFFREY T. SMITH, and KAREN M. HASTINGS, *Administrative Patent Judges*.

WALTZ, *Administrative Patent Judge.*

DECISION ON APPEAL

This is a decision on an appeal under 35 U.S.C. § 134 from the Primary Examiner's final rejection of claims 1-11, which are the only claims pending in this application. We have jurisdiction pursuant to 35 U.S.C. § 6(b).

According to Appellants, the invention is directed to a process for fabricating bumps with different size and height, where a photoresist layer is

formed over a wafer having a plurality of bonding pads and a passivation layer thereon, with the passivation layer exposing the bonding pads and the photoresist layer having a plurality of openings with different widths positioned corresponding to the bonding pads (App. Br. 1-2). Appellants use an increasing step current composed of several current pulses to control deposition of metal ions from an electrolytic solution into the narrow openings (App. Br. 2). Further details of the invention may be gleaned from illustrative independent claim 1, as reproduced below:

> 1. A process for fabricating bumps, comprising the steps of: providing a wafer having a plurality of bonding pads and a passivation layer thereon, wherein the passivation layer is disposed on a surface of the wafer and exposes the bonding pads; forming a photoresist layer over the wafer, wherein the photoresist layer has a plurality of openings with different widths and the openings are positioned corresponding to the bonding pads; immersing the wafer into an electrolytic solution; and performing an electroplating operation by providing an increasing step current to the electrolytic solution.

The Examiner has relied on the following prior art references as evidence of obviousness:

Ihara	6,030,512	Feb. 29, 2000
Chung	6,409,903 B1	Jun. 25, 2002
Jao	6,415,974 B2	Jul. 9, 2002
Bojkov	2004/0140219 A1	Jul. 22, 2004

ISSUE ON APPEAL

Claims 1-10 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Bojkov in view of Chung and Jao (Ans. 3). Claim 11 stands rejected under § 103(a) as unpatentable over the references as applied against claims 1-10, further in view of Ihara (Ans. 7).

Appellants contend that Bojkov fails to disclose the increasing step current for openings with different widths and requires a relaxation period as an essential element (App. Br. 5).

Appellants contend that Chung clearly shows that the reason for ramping up the current to a constant current value without exceeding the threshold voltage is to prevent the seed layer on the wafer from burn-through (App. Br. 5). Appellants also contend that neither Bojkov nor Chung raise the issue of forming the bumps by using the photoresist layer having a plurality of openings with different widths (App. Br. 6). Appellants further contend that Jao points to an issue similar to what has been discussed in the present invention, but provides a different solution to the problem (App. Br. 6-7).

Appellants contend that even if combined, the combination of references would "jeopardize" Bojkov's application, since using the ramping current of Chung would not allow for the essential relaxation periods required by Bojkov (App. Br. 6, 8).[1]

The Examiner contends that Bojkov discloses all the limitations of claim 1 on appeal with the exception of a substrate in the form of a wafer, the openings having different widths, and increasing the current (Ans. 3-4). The Examiner further contends that Jao teaches the benefits of forming bumps in a plurality of openings with various sizes, although Appellants admit that electroplating bumps having different widths is conventional in

[1] Appellants state that claims 1-11 may be treated as one group to stand or fall together, with independent claim 1 taken as representative for the issues on appeal (App. Br. 3). *See* 37 C.F.R. § 41.37(c)(1)(vii). We note that Appellants present arguments concerning the rejection of claim 11, but these arguments are the same as provided against claim 1 (App. Br. 7-8).

the art (Ans. 4, 8, and 9). The Examiner also contends that Chung teaches a method for providing a uniform electroplated surface while minimizing "burn-through" of the seed layer used on the substrate to initiate electroplating by ramping up to a current value from a first current value (Ans. 4).

From the record presented in this appeal, we determine the following issue: have Appellants established that the Examiner committed reversible error in combining the applied prior art references to establish obviousness under § 103(a)? We answer this question in the negative for the reasons stated in the Answer, as well as those reasons set forth below. Therefore, we AFFIRM all grounds of rejection presented for review in this appeal.

OPINION

We determine the following Factual Findings (FF) from the record in this appeal:

(1) Bojkov discloses a process for fabricating bumps comprising the steps of providing a semiconductor substrate having a plurality of bonding pads and a passivation layer thereon, where the passivation layer is disposed on a surface of the substrate and exposes the bonding pads; forming a photoresist layer over the substrate, where the photoresist layer has a plurality of openings positioned corresponding to the bonding pads; immersing the substrate into an electrolytic solution; and performing an electroplating operation by providing a step current to the electrolytic solution (Ans. 3-4; Bojkov, Abstract; Fig. 2A; ¶¶ [0013], [0014], [0018], [0019], and [0020]);

(2) Bojkov teaches that electrical current is passed through the electrolytic solution so as to cause the conductive material to deposit on the substrate, where the level of electrical current is varied from a first current level to a second current level, and the second current level may be at a rate slower or faster than the first current level, with an embodiment where the second current level provides a relaxation period to allow the conductive material deposited on the substrate to come to equilibrium (Ans. 4; Bojkov, Abstract; ¶¶ [0005], [0006], [0015], [0021], [0022] and [0024]);

(3) Bojkov teaches, in one particular embodiment, that the low second current level may be increased to a third current level by controller 26, and that the current from current source 24 may be pulsed (Bojkov, ¶¶ [0023], [0025], and [0032]);

(4) Bojkov discloses a seed layer 44 which may comprise under-bump metallurgy (UBM), with a primary purpose of adhering to the inner conductive layer 40 and providing a nucleation layer for electroplated film (Bojkov, ¶ [0019]);

(5) Chung discloses a method for the electroplating of a substrate such as a semiconductor wafer which provides a uniform electroplated surface and minimizes "burn-through" of the seed layer used to initiate electroplating by use of a multistep electroplating process (Ans. 4; Chung, Abstract; col. 1, ll. 5-11 and 47-60; col. 3, ll. 49-54);

(6) Chung teaches plating onto the seed layer with a current pre-programmed to ramp up to a current value from a first current value, using several steps of increasing the current over time to a

final high value current where the threshold voltage is not exceeded and there is no "burn-through" (Ans. 4; Chung, Abstract; col. 2, ll. 40-45; col. 3, ll. 6-10; col. 7, ll. 5-17; Fig. 4 and col. 7, ll. 54-56);

(7) Jao discloses a structure with a plurality of solder bumps where the UBM structure has various sizes of openings to control the volume of the solder in order to form uniform heights of the solder bumps (Ans. 4; Jao, Abstract; Figs. 1A and 3A; col. 1, ll. 38-42; col. 2, ll. 15-29 and 39-43; col. 3, ll. 1-28 and 37-47; col. 4, ll. 52-54; col. 5, ll. 14-15, 30-32, and 39-41).

(8) Appellants disclose that the openings in the photoresist layer are often designed to have different widths (Spec., ¶ [0007]), exemplifying this conventional practice in Fig. 1 labeled as "Prior Art".

Under 35 U.S.C. § 103, the factual inquiry into obviousness requires a determination of: (1) the scope and content of the prior art; (2) the differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) secondary considerations, if any. *See Graham v. John Deere Co.,* 383 U.S. 1, 17-18 (1966). "[I]f a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill." *KSR Int'l Co. v. Teleflex, Inc.,* 127 S. Ct. 1727, 1740 (2007). "Under the correct analysis, any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed." *KSR,* 127 S. Ct.

at 1741. It is axiomatic that admitted prior art in an applicant's specification may be used in determining the patentability of the claimed invention. *See In re Nomiya,* 509 F.2d 566, 570-71 (CCPA 1975). Consideration of the prior art cited by the Examiner may include consideration of the admitted prior art found in an applicant's specification. *See In re Davis,* 305 F.2d 501, 503 (CCPA 1962); *cf., In re Hedges,* 783 F.2d 1038, 1039-40 (Fed. Cir. 1986).

Applying the preceding legal principles to the Factual Findings (FF) from the record in this appeal, we determine that the Examiner has established a prima facie case of obviousness in view of the reference evidence, which prima facie case has not been adequately rebutted by Appellants' arguments. As shown by FFs (1), (2), and (3) listed above, we determine that Bojkov discloses every limitation of claim 1 on appeal, including the use of an increasing step current (*see* FF (3)), with the exception of using openings in the photoresist layer with different widths. As shown by FF (5) and (6) listed above, we determine that Chung teaches the "ramping" up of current in steps, as does Bojkov, but employs these current values to solve the problem of "burn-through" in the seed layer. As shown by FF (4) listed above, we determine that Bojkov also teaches use of a seed layer to help initiate electroplating. As shown by FF (7) and (8) listed above, we determine that the use of openings in the photoresist layer of different widths was well known in the art, with advantages of forming uniform heights of the solder bumps. Accordingly, we determine that it would have been well within the ordinary skill in the art at the time of Appellants' invention to have used openings with different widths in the photoresist layer, as taught by Jao and admitted as conventional by

Appellants, in the process disclosed by Bojkov. Similarly, we determine that the use of an increasing step current, as taught by Bojkov or Chung, would have been obvious in the process of Bojkov to eliminate or reduce burn-through.

Appellants argue that Bojkov fails to disclose increasing step current for openings of different widths and requires a relaxation period as an essential element (App. Br. 5-6 and 8). This argument is not persuasive since Jao and Appellants' admission have been used by the Examiner as evidence of the conventionality and advantages of using openings in the photoresist layer having different widths (Ans. 8-9). As discussed above, both Bojkov and Chung teach the use of increasing step currents during the electroplating process (*see* FF (3) and (6)). Contrary to Appellants' argument (App. Br. 6, 8), the presence of a relaxation period, as taught by Bojkov, would not affect the combination of references. *See* FF (3) listed above, where Bojkov teaches that the low current step, which may be the relaxation period, may be followed by a step of increasing the current to a third level.

Appellants argue that Chung gives a reason for ramping up the current (prevention of "burn-through" on the seed layer), implying that this reason is different than the reason of Appellants for increasing the current (App. Br. 5). However, the reason for combining the prior art does not have to be the same as Appellants' reason. *See KSR,* 127 S. Ct. at 1741 ("Under the correct analysis, any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.").

Appellants argue that only Jao raises the issue of forming bumps with different width openings, and Jao provides a different solution to this problem (App. Br. 6-7). This argument is not well taken since Appellants admit that using different width openings in the photoresist layer was conventional (*see* FF (8)). Furthermore, Jao teaches the benefits or advantages of employing different widths in the openings of the photoresist layer (*see* FF (7)).

For the foregoing reasons and those stated in the Answer, we sustain the rejection of claim 1 (and claims 2-10 which stand or fall with claim 1) under § 103(a) over Bojkov in view of Chung and Jao. Since Appellants have not presented any separate arguments concerning the rejection of claim 11 (App. Br. 3), we adopt the Examiner's factual findings and conclusion of law concerning this rejection (Ans. 7), and also sustain this rejection.[2] The decision of the Examiner is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

tc

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[2] Thus a discussion of Ihara is unnecessary to this decision.